WHAT IS CLAIMED IS:

1. A signal processing circuit generating a digital signal based on an input pulse signal, the signal processing circuit comprising:

a clock pulse output circuit which outputs clock pulses having one of positive and negative polarities for a period which includes a pulse of the input pulse signal;

a counter circuit which counts the clock pulses; and

an output circuit which outputs the digital signal based on a counted value of said counter circuit.

2. The signal processing circuit as claimed in claim 1, wherein:

said clock pulse output circuit comprises:

a first clock pulse output circuit which outputs clock pulses when the input pulse signal has a positive polarity; and

a second clock pulse output circuit which outputs clock pulses when the input pulse signal has a negative polarity; and

said counter circuit comprises:

a first counter circuit which counts the clock pulses supplied from said first clock pulse output circuit; and

a second counter circuit which counts the clock

pulses supplied from said second clock pulse output circuit.

3. The signal processing circuit as claimed in claim 2, wherein:

said first counter circuit outputs a first timing signal at a first predetermined counted value;

said second counter circuit outputs a second timing signal at a second predetermined counted value; and

said output circuit comprises:

a first latch circuit which latches a counted value of said first counter circuit based on the second timing signal; and

a second latch circuit which latches a counted value of said second counter circuit based on the first timing signal.

4. The signal processing circuit as claimed in claim 3, wherein:

said output circuit comprises:

a first delay circuit which delays the first timing signal; and

a second delay circuit which delays the second timing signal;

said first counter circuit is reset by an output signal of said second delay circuit; and

said second counter circuit is reset by an output

signal of said first delay circuit.

5. The signal processing circuit as claimed in claim 4, wherein said output circuit further comprises:

a flip flop which is set by the output signal of said first delay circuit and is reset by the output signal of said second delay circuit; and

a switching circuit which switches, based on an output of said flip flop, between outputs of the counted values latched by said first and second latch circuits, respectively.

6. The signal processing circuit as claimed in claim 2, wherein said counter circuit further comprises:

a third counter circuit which counts the clock pulses supplied from said first clock pulse output circuit;

a fourth counter circuit which counts the clock pulses supplied from said second clock pulse output circuit; and

a setting circuit which sets the predetermined period based on respective predetermined counted values of said third and fourth counter circuits.

7. The signal processing circuit as claimed in claim 6, wherein:

said third counter circuit outputs a first timing signal at the predetermined counted value of said third counter circuit;

said fourth counter circuit outputs a second timing signal at the predetermined counted value of said fourth counter circuit; and

said setting circuit outputs, based on the first and second timing signals, a signal which determines the predetermined period.

8. The signal processing circuit as claimed in claim 7, wherein said setting circuit comprises a flip flop which is set by the first timing signal and is reset by the second timing signal.

9. The signal processing circuit as claimed in claim 8, wherein one of the counted values of said third and fourth counter circuits is reset when said flip flop is reset.

10. The signal processing circuit as claimed in claim 8, wherein said output circuit comprises:

a rising edge output circuit which outputs a third timing signal at a rising edge of an output of said flip flop;

a falling edge output circuit which outputs a fourth timing signal at a falling edge of the output of said flip flop;

a first latch circuit which latches a counted value of said first counter circuit based on the fourth timing signal; and

a second latch circuit which latches a counted value of said second counter circuit based on the third timing signal.



11. The signal processing circuit as claimed in claim 10, wherein:

said output circuit further comprises:

a first delay circuit which delays the third timing signal and outputs a fifth timing signal; and

a second delay circuit which delays the fourth timing signal and outputs a sixth timing signal;

said first counter circuit is reset by the sixth timing signal; and

said second counter circuit is reset by the fifth timing signal.

12. The signal processing circuit as claimed in claim 10, wherein said output circuit further comprises a

switching circuit which switches, based on an output of said flip flop, between outputs of the counted values latched by said first and second latch circuits, respectively.

13. The signal processing circuit as claimed in claim 2, wherein said output circuit comprises:

a generation circuit which generates a phase difference pulse signal having a predetermined phase difference with respect to the input pulse signal;

a rising edge output circuit which outputs a third timing signal at a rising edge of the phase difference pulse signal;

a falling edge output circuit which outputs a fourth timing signal at a falling edge of the phase difference pulse signal;

a first latch circuit which latches a counted value of said first counter circuit based on the third timing signal; and

a second latch circuit which latches a counted value of said second counter circuit based on the fourth timing signal.

14. The signal processing circuit as claimed in claim 13, wherein:

said output circuit further comprises:

a first delay circuit which delays the third

timing signal to output a fifth timing signal; and

a second delay circuit which delays the fourth timing signal to output a sixth timing signal;

said first counter circuit is reset by the fifth timing signal; and

said second counter circuit is reset by the sixth timing signal.

15. The signal processing circuit as claimed in claim 13, wherein said output circuit further comprises:

a third delay circuit which delays the phase difference pulse signal to output a delayed phase difference pulse signal; and

a switching circuit which switches, based on the delayed phase difference pulse signal, between outputs of the counted values latched by said first and second latch circuits, respectively.

16. The signal processing circuit as claimed in claim 1, wherein said output circuit includes a digital low-pass filter.

17. A method of generating a digital signal based on an input pulse signal, the method comprising the

steps of:

(a) outputting clock pulses having one of positive and negative polarities for a period including a pulse of the input pulse signal;

(b) counting the clock pulses; and

(c) outputting the digital signal based on the counted value obtained in said step (b).